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10/603,273	06/25/2003	Peter Brandt	31021037 US-01	4469

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Paul D. Greeley, Esq.
Ohlandt, Greeley, Ruggiero & Perle, L.L.P.
10th Floor
One Landmark Square
Stamford, CT 06901-2682

EXAMINER	
DWIVEDI, MAHESH H	
ART UNIT	**PAPER NUMBER**
2168	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,273	BRANDT, PETER	
	Examiner	Art Unit	
	Mahesh H. Dwivedi	2168	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-29,32,34 and 36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-29,32,34 and 36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/28/2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Receipt of Applicant's Amendment, filed on 08/27/2007, is acknowledged. The amended parts includes the amending of claims 16-17, 22-23, 26, 29, 32, and 34, the cancellation of claims 1-15, 30-31, 33, 35, and 37.

Claim Objections

2. The objections raised in the office action mailed on 04/05/2007 have been overcome by applicant's amendments received on 08/27/2007.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 16-24, 26-27, 29, 32, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Boner** (U.S. Patent 6,625,763) in view of **Hemming** (U.S. PGPUB 2004/0168011).

5. Regarding claim 16 **Boner** teaches a method comprising:

B) inputting a stream of data entities in a serial format into a shift register that shift said data entities therethrough and reformats said data entities from said serial format into a parallel format (Column 6, lines 24-38, lines 39-51),

C) writing said data entities, in said parallel format, from said shift register said memories (Column 6, lines 39-51, Figures 5-11);

D) performing selection and permutation on said memories (Column 8, lines 23-33, lines 35-39), and

E) Reading out said data entities in said permuted memories, in a memory-by-memory fashion (Column 8, lines 23-33, Figures 3-11).

The examiner notes that **Boner** teaches **"inputting a stream of data entities in a serial format into a shift register that shift said data entities therethrough and**

reformats said data entities from said serial format into a parallel format" as "Block interleaver 300 operates as follows. The first sixteen data values D_0- D_{15} are written to register file 301 in column order. Thus, during a first 4-bit write operation, the first four data values D_0- D_3 are written to memory cells M_0, M_4, M_8 and M_{12}, respectively, through the first ports (P1) of these memory cells. This pattern continues, with the next four data values D_4- D_7 being written through the first ports of memory cells M_1, M_5, M_9 and M_{13}, respectively, during a second 4-bit write operation. The next four data values D_8- D_{11} are then written through the first ports of memory cells M_2, M_6, M_{10} and M_{14}, respectively, during a third 4-bit write operation. The next four data values D_{12}- D_{15} are then written through the first ports of memory cells M_3, M_7, M_{11} and M_{15}, respectively, during a fourth 4-bit write operation. Four 4-bit write operations must therefore be performed to fill register file 301 as illustrated in FIG. 3" (Column 6, lines 24-38) and "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46). The examiner further notes that **Boner** teaches **"writing said data entities, in said parallel format, from said shift register said memories"** as "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46). The examiner further notes that **Boner** teaches **"performing selection and permutation on said memories"** as "permutations in the column order can be accommodated, by changing the manner in which data is transferred from register file 301 to Ram 200" (Column 8, lines 23-26) and "register file 301 can be implemented as a single-port RAM that can be written in column order" (Column 8, lines 35-39). The

examiner further notes that the register file of **Boner** is a form of memory, and permutations are performed on the register file.

Boner does not explicitly teach:

A) providing a number of memories equal to the maximum number of columns in the interleaving function.

Hemming, however, teaches **"providing a number of memories equal to the maximum number of columns in the interleaving function"** as "the interleaver comprises four RAM devices M1 to M4 and sixteen register memories to store sixteen data values or symbols B1-to B4, C1 to C4, D1 to D4, and E1 to E4" (Paragraph 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hemming's** would have allowed **Boner's** to provide accessing memories linearly without requiring multiport memory devices with several reading ports, as noted by **Hemming** (Paragraph 14).

Regarding claim 17, **Boner** further teaches a method comprising:

A) wherein said writing is applied when said shift register is filled (Column 6, lines 39-46).

The examiner notes that **Boner** teaches **"wherein said writing is applied when said shift register is filled"** "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46).

Regarding claim 18, **Boner** further teaches a method comprising:

A) wherein said data entities are logical ones and zeros (Column 5, lines 17-19, Figure 2).

The examiner notes that Boner teaches **"wherein said data entities are logical ones and zeros"** as "a 4 column by 32 row RAM 200, which stored sequential data bits D0-D127 in a column order" (Column 5, lines 17-19). The examiner further notes that it is common knowledge that "data bits" (Column 5, lines 18) are in binary form.

Regarding claim 19, **Boner** further teaches a method comprising:

A) wherein said data entities are multiple bit words (Column 2, lines 31-45, Column 3, lines 40-45, Figures 3-11).

The examiner notes that Boner teaches **"wherein said data entities are multiple bit words"** as "If the SRAM block interleaver is arranged so that each row stores one or more memory words" (Column 2, lines 35-36).

Regarding claim 20, **Boner** further teaches a method comprising:

A) wherein said data entities are three bit words (Column 2, lines 43-45).

The examiner notes that Boner teaches **"wherein said data entities are three bit words"** as "assuming a word length of 3 bits (a full row), the block interleaver will be written during four cycles" (Column 2, lines 43-45).

Regarding claim 21, **Boner** further teaches a method comprising:

A) wherein said register is arranged to store each multiple bit word at one location in said memories (Column 3, lines 48-59.

The examiner notes that Boner teaches **"wherein said register is arranged to store each multiple bit word at one location in said memories"** as "the data values are written to the interleaver RAM in a row order, which is selected to implement a permutation of a column order of the original data stream" (Column 3, lines 49-52).

Regarding claim 22, **Boner** further teaches a method comprising:

A) wherein a number of columns used in said column interleaver function is changed on the fly, and wherein said number of columns does not exceed said maximum number of columns (Column 1, lines 54-60, Column 4, lines 14-19, lines 54-57).

The examiner notes that the interleaving function taught by **Boner** can be used for different bit sizes with accompanying columns.

Regarding claim 23 **Boner** teaches a module comprising:

B) a shift register that receives a stream of data entities in a serial format, shifts said data entities therethrough, and reformats said data entities from said serial format into a parallel format (Column 6, lines 24-38, lines 39-51); and

C) a controller that controls writing said data entities, in said parallel format, from said shift register into said memories (Column 6, lines 39-51, Figures 5-11); and

D) selection and permutation on said memories (Column 8, lines 23-33, lines 35-39); and

E) reading out said data entities in said permuted memories, in a memory-by-memory fashion (Column 8, lines 23-33, Figures 3-11).

The examiner notes that **Boner** teaches **"a shift register that receives a stream of data entities in a serial format, shifts said data entities therethrough, and reformats said data entities from said serial format into a parallel format"** as "Block interleaver 300 operates as follows. The first sixteen data values D_0- D_{15} are written to register file 301 in column order. Thus, during a first 4-bit write operation, the first four data values D_0- D_3 are written to memory cells M_0, M_4, M_8 and M_{12}, respectively, through the first ports (P1) of these memory cells. This pattern continues, with the next four data values D_4- D_7 being written through the first ports of memory cells M_1, M_5, M_9 and M_{13}, respectively, during a second 4-bit write operation. The next four data values D_8- D_{11} are then written through the first ports of memory cells M_2, M_6, M_{10} and M_{14}, respectively, during a third 4-bit write operation. The next four data values D_{12}- D_{15} are then written through the first ports of memory cells M_3, M_7, M_{11} and M_{15}, respectively, during a fourth 4-bit write operation. Four 4-bit write operations must therefore be performed to fill register file 301 as illustrated in FIG. 3" (Column 6, lines 24-38) and "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register

file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46). The examiner further notes that **Boner** teaches **"a controller that controls writing said data entities, in said parallel format, from said shift register into said memories"** as "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46). The examiner further notes that **Boner** teaches **"selection and permutation on said memories"** as "permutations in the column order can be accommodated, by changing the manner in which data is transferred from register file 301 to Ram 200" (Column 8, lines 23-26) and "register file 301 can be implemented as a single-port RAM that can be written in column order" (Column 8, lines 35-39). The examiner further notes that the register file of **Boner** is a form of memory, and permutations are performed on the register file.

Boner does not explicitly teach:

A) a number of memories equal to a maximum number of columns in a interleaving function.

Hemming, however, teaches **"a number of memories equal to a maximum number of columns in a interleaving function"** as "the interleaver comprises four RAM devices M1 to M4 and sixteen register memories to store sixteen data values or symbols B1-to B4, C1 to C4, D1 to D4, and E1 to E4" (Paragraph 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hemming's** would have allowed **Boner's** to provide accessing memories linearly without requiring multiport memory devices with several reading ports, as noted by **Hemming** (Paragraph 14).

Regarding claim 24, **Boner** teaches a module comprising:

A) A communication system device (Column 1, lines 14-20).

Regarding claim 26 **Boner** teaches an integrated circuit device comprising:

B) a shift register that receives a stream of data entities in a serial format, shifts said data entities therethrough, and reformats said data entities from said serial format into a parallel format (Column 6, lines 24-38, lines 39-51); and

C) a sub-circuit that controls writing said data entities successively from said shift register into a memory, until all memories are completely filled or until all data entities are written (Column 6, lines 39-51, Figures 5-11); and

D) selection and permutation on said memories (Column 8, lines 23-33, lines 35-39); and

E) reading out said data entities in said permuted memories, in a memory-by-memory fashion (Column 8, lines 23-33, Figures 3-11).

The examiner notes that **Boner** teaches **"a shift register that receives a stream of data entities in a serial format, shifts said data entities therethrough, and reformats said data entities from said serial format into a parallel format"** as "Block interleaver 300 operates as follows. The first sixteen data values D_0- D_{15} are written to register file 301 in column order. Thus, during a first 4-bit write operation, the first four data values D_0- D_3 are written to memory cells M_0, M_4, M_8 and M_{12}, respectively, through the first ports (P1) of these memory cells. This pattern continues, with the next four data values D_4- D_7 being written through the first ports of memory cells M_1, M_5, M_9 and M_{13}, respectively, during a second 4-bit write operation. The next four data values D_8- D_{11} are then written through the first ports of memory cells M_2, M_6, M_{10} and M_{14}, respectively, during a third 4-bit write operation. The next four data values D_{12}- D_{15} are then written through the first ports of memory cells M_3, M_7, M_{11} and M_{15}, respectively, during a fourth 4-bit write operation. Four 4-bit write operations must therefore be performed to fill register file 301 as illustrated in FIG. 3" (Column 6, lines 24-38) and "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24,

respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46). The examiner further notes that **Boner** teaches **"a sub-circuit that controls writing said data entities, in said parallel format, from said shift register into said memories"** as "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46). The examiner further notes that **Boner** teaches **"selection and permutation on said memories"** as "permutations in the column order can be accommodated, by changing the manner in which data is transferred from register file 301 to Ram 200" (Column 8, lines 23-26) and "register file 301 can be implemented as a single-port RAM that can be written in column order" (Column 8, lines 35-39). The examiner further notes that the register file of **Boner** is a form of memory, and permutations are performed on the register file.

Boner does not explicitly teach:

A) a number of memories equal to a maximum number of columns in a interleaving function.

Hemming, however, teaches **"a number of memories equal to a maximum number of columns in a interleaving function"** as "the interleaver comprises four RAM devices M1 to M4 and sixteen register memories to store sixteen data values or symbols B1-to B4, C1 to C4, D1 to D4, and E1 to E4" (Paragraph 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hemming's** would have allowed **Boner's** to provide accessing memories linearly without requiring multiport memory devices with several reading ports, as noted by **Hemming** (Paragraph 14).

Regarding claim 27, **Boner** teaches an integrated circuit comprising:

A) A communication system device (Column 1, lines 14-20).

Regarding claim 29 **Boner** teaches a column interleaver comprising:

B) a shift register that receives a stream of data entities in a serial format said data entities therethrough, and reformats said data entities from said serial format into a parallel format (Column 6, lines 24-38, lines 39-51); and

C) a module that controls (a) writing of said data entities in said parallel format from said shift register to said memories (Column 6, lines 39-51, Figures 5-11); and

D) column selection and permutation (Column 8, lines 23-33, lines 35-39).

The examiner notes that **Boner** teaches **"a shift register that receives a stream of data entities in a serial format said data entities therethrough, and reformats said data entities from said serial format into a parallel format"** as "Block interleaver 300 operates as follows. The first sixteen data values D_0- D_{15} are written to register file 301 in column order. Thus, during a first 4-bit write operation, the first four data values D_0- D_3 are written to memory cells M_0, M_4, M_8 and M_{12}, respectively, through the first ports (P1) of these memory cells. This pattern continues, with the next four data values D_4- D_7 being written through the first ports of memory cells M_1, M_5, M_9 and M_{13}, respectively, during a second 4-bit write operation. The next four data values D_8- D_{11} are then written through the first ports of memory cells M_2, M_6, M_{10} and M_{14}, respectively, during a third 4-bit write operation. The next four data values D_{12}- D_{15} are then written through the first ports of memory cells M_3, M_7, M_{11} and M_{15}, respectively, during a fourth 4-bit write operation. Four 4-bit write operations must therefore be performed to fill register file 301 as illustrated in FIG. 3" (Column 6, lines 24-38) and "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data

bits within the interleaved data stream" (Column 6, lines 39-46). The examiner further notes that **Boner** teaches **"a module that controls (a) writing of said data entities in said parallel format from said shift register to said memories"** as "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46). The examiner further notes that **Boner** teaches **"column selection and permutation"** as "permutations in the column order can be accommodated, by changing the manner in which data is transferred from register file 301 to Ram 200" (Column 8, lines 23-26) and "register file 301 can be implemented as a single-port RAM that can be written in column order" (Column 8, lines 35-39).

Boner does not explicitly teach:

A) a number of memories equal to a maximum number of columns desired in said column interleaver.

Hemming, however, teaches **"a number of memories equal to a maximum number of columns desired in said column interleaver"** as "the interleaver comprises four RAM devices M1 to M4 and sixteen register memories to store sixteen data values or symbols B1-to B4, C1 to C4, D1 to D4, and E1 to E4" (Paragraph 29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hemming's** would have allowed **Boner's** to provide accessing memories linearly without requiring multiport memory devices with several reading ports, as noted by **Hemming** (Paragraph 14).

Regarding claim 32, **Boner** further teaches a module comprising:

A) wherein said controller controls said writing to occur when said shift register is filled (Column 6, lines 39-46).

The examiner notes that **Boner** teaches **"wherein said controller controls said writing to occur when said shift register is filled"** "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46).

Regarding claim 34, **Boner** further teaches an integrated circuit device comprising:

A) wherein said sub-controller controls said writing to occur when said shift register is filled (Column 6, lines 39-46).

he examiner notes that **Boner** teaches **"wherein said sub-controller controls said writing to occur when said shift register is filled"** "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46).

Regarding claim 36, **Boner** further teaches a column interleaver comprising:

A) wherein said module controls said writing to occur when said shift register is filled (Column 6, lines 39-46).

The examiner notes that **Boner** teaches **"wherein said module controls said writing to occur when said shift register is filled"** "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations

to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46).

6. Claims 25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Boner** (U.S. Patent 6,625,763) in view of **Hemming** (U.S. PGPUB 2004/0168011) as applied to claims 16-24, 26-27, 29, 32, 34, and 36, and further in view of **Hustig et al.** (U.S. Patent 4,672,605).

7. Regarding claim 25, **Boner** and **Hemming** do not explicitly teach a module comprising:

A) A spread-spectrum communication apparatus

Hustig, however teaches "spread-spectrum communication apparatus" as "spread spectrum techniques" (Column 3, lines 38-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hustig's** would have allowed **Boner's** and **Hemming's** to provide error free communication, as noted by **Hustig** (Column 1, lines 55-57).

Regarding claim 28, **Boner** and **Hemming** do not explicitly teach an integrated circuit device comprising:

A) A spread-spectrum communication apparatus

Hustig, however teaches "spread-spectrum communication apparatus" as "spread spectrum techniques" (Column 3, lines 38-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of the cited references because teaching **Hustig's** would have allowed **Boner's** and **Hemming's** to provide error free communication, as noted by **Hustig** (Column 1, lines 55-57).

Response to Arguments

8. Applicant's arguments filed on 08/27/2007 have been fully considered but they are not persuasive.

Applicants argue on page 07 that **"the Boner patent does not describe register 301 as having any data shifted therethrough"** and specifically that **"the Boner patent does not disclose inputting a stream of data entities in a serial format into a shift register that shifts the data entities therethrough and reformats the data entities from the serial format into a parallel format"**. However, the examiner wishes to refer to Column 6 of **Boner** which states "Block interleaver 300 operates as follows. The first sixteen data values D_0- D_{15} are written to register file 301 in column order. Thus, during a first 4-bit write operation, the first four data values D_0- D_3 are written to memory cells M_0, M_4, M_8 and M_{12}, respectively, through the first ports (P1) of these memory cells. This pattern continues, with the next four data values D_4- D_7 being written through the first ports of memory cells M_1, M_5, M_9 and M_{13}, respectively, during a second 4-bit write operation. The next four data values D_8- D_{11} are then written through the first ports of memory cells M_2, M_6, M_{10} and M_{14}, respectively, during a third 4-bit write operation. The next four data values D_{12}- D_{15} are then written through the first ports of memory cells M_3, M_7, M_{11} and M_{15}, respectively, during a fourth 4-bit write operation. Four 4-bit write operations must therefore be performed to fill register file 301 as illustrated in FIG. 3" (Column 6, lines 24-38) and "After register file 301 has been filled, the 4-bit values stored in rows R0, R1, R2 and R3 of register file 301 are transferred to rows R0, R8, R16 and R24, respectively, of RAM 200. This process requires four 4-bit read operations from register file 301 and four 4-bit write operations to RAM 200. The four write operations to RAM 200 are staggered by eight rows, thereby promoting the separation of consecutive data bits within the interleaved data stream" (Column 6, lines 39-46). The examiner further wishes to state that the instant specification of the instant application does not define nor explain what serial and parallel constitute. The entirely short and broad specification merely states the terms without explaining what they specifically entail. Because of the nonexistent definitions of serial and parallel, the examiner interprets serial as reading a stream of data in order. Moreover, the examiner interprets parallel as writing to non-consecutive storage areas simultaneously. In **Boner**, the stream of data entities are written in order (i.e. serially) (see "The first sixteen data values D_0- D_{15} are written to register file 301 in column

order. Thus, during a first 4-bit write operation, the first four data values D_0- D_3 are written to memory cells", where D_0- D_{15} are written consecutively. Furthermore, in **Boner**, the register file then transfers, via row order, the input into non-consecutive memories.

Applicants argue on page 08 that **"in the Boner patent...are written to register file in parallel and data values...are written to Ram 200 in serial format"**. However, as previously discussed, the in **Boner**, the data entities are written serially and read out in parallel.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,954,885 issued to **Hurt et al.** on 11 October 2005. The subject matter disclosed therein is pertinent to that of claims 16-29, and 32, 34, and 36 (e.g., methods interleave data).

U.S. Patent 6,061,820 issued to **Nakakita et al.** on 09 May 2000. The subject matter disclosed therein is pertinent to that of claims 16-29, 32, 34, and 36 (e.g., methods interleave data).

U.S. Patent 6,631,491 issued to **Shibutani et al.** on 07 October 2003. The subject matter disclosed therein is pertinent to that of claims 16-29, 32, 34, and 36 (e.g., methods interleave data).

U.S. Patent 4,291,406 issued to **Bahl et al.** on 22 September 1981. The subject matter disclosed therein is pertinent to that of claims 16-29, 32, 34, and 36 (e.g., methods interleave data).

U.S. Patent 4,394,642 issued to **Currie et al.** on 19 July 2003. The subject matter disclosed therein is pertinent to that of claims 16-29, 32, 34, and 36 (e.g., methods interleave data).

U.S. Patent 7,127,004 issued to **Sönning et al.** on 04 October 2006. The subject matter disclosed therein is pertinent to that of claims 16-29, 32, 34, and 36 (e.g., methods interleave data).

U.S. Patent 5,022,029 issued to **Guichon** on 04 June 1991. The subject matter disclosed therein is pertinent to that of claims 16-29, 32, 34, and 36 (e.g., methods interleave data).

U.S. Patent 6,353,900 issued to **Sindhushayana et al.** on 05 March 2002. The subject matter disclosed therein is pertinent to that of claims 16-29, 32, 34, and 36 (e.g., methods interleave data).

U.S. Patent 6,334,197 issued to **Eroz et al.** on 25 December 2001. The subject matter disclosed therein is pertinent to that of claims 16-29, 32, 34, and 36 (e.g., methods interleave data).

U.S. Patent 6,035,427 issued to **Kweon** on 07 March 2000. The subject matter disclosed therein is pertinent to that of claims 16-29, 32, 34, and 36 (e.g., methods interleave data).

U.S. Patent 5,719,975 issued to **Wei** on 17 February 1998. The subject matter disclosed therein is pertinent to that of claims 16-29, 32, 34, and 36 (e.g., methods interleave data).

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mahesh Dwivedi whose telephone number is (571) 272-2731. The examiner can normally be reached on Monday to Friday 8:20 am – 4:40 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Vo can be reached (571) 272-3642. The fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mahesh Dwivedi
Patent Examiner
Art Unit 2168

November 07, 2007

TIM VO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100